CURRENT-VOLTAGE CHARACTERISTICS, SMALL-SIGNAL PARAMETERS, SWITCHING TIMES AND POWER-DELAY PRODUCTS OF GaAs MESFET's.

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ABSTRACT

New simple computer and analytical models of GaAs MESFET's are proposed. The models are based on the assumption that the current saturation in GaAs MESFETs is related to the stationary Gunn domain formation at the drain side of the gate rather than to a pinch-off of the conducting channel under the gate. The results of the calculation are in good agreement with experimental data. The models can be used for a computer-aided design of GaAs integrated circuits.

Introduction

We describe two models of a GaAs MESFET (computer and analytical) which are very suitable for the applications in the computer-aided design. We also present the current-voltage characteristics, small-signal parameters, power-delay products, switching times of GaAs FETs calculated in the frame of these two models and compare them with the results of previous computer calculations and experimental data.

Both our models may be considered as a compromise between a simple qualitative description of FETs provided by the Shockley theory and a rigorous computer analysis. The Shockley theory gives a physical insight into FET's operation but fails to provide a reasonable agreement with experimental data because the hot electron effects are not adequately included. A rigorious two-dimensional analysis, on the other hand, requires a very large computer time and that is why it is hardly suitable for a computer-aided design.

Our computer model requires a very small computation time (0.2 sec per point of current-voltage characteristic) but it is based on the physical picture revealed by a rigorous two-dimensionsal computer analysis and takes into account the diffusion processes and the Gunn domain formation at the drain side of the gate. For the analytical model we use the standart Shockley theory of FETs to describe the section under the gate and the analytic theory of Gunn domain in high-doped semiconductors developed by Gelmont and Shur [1]. The saturation current, channel conductance, transconductance, charge under the gate, gate-to-source and drain-to-gate capacitances, cut-off frequency, characteristic switching time, power-delay product and breakdown voltage are calculated in the frame of these models. The results agree well with the results of the computer analysis and experimental data for a 1 μm gate GaAs MESFET.

Description of the models and analytical results

The main features of the computer model are

1) It divides the MESFET into three sections (a) source-gate portion which is assumed to behave like an ohmic resistance (b) a channel under the gate, and (c) adjacent Gunn domain, extending toward the drain, which can form if the electric field at the drain side of the channel is larger than a sustaining domain field. In this aspect the model is similar to one developed by Engelmann and Liechti [2].

2) The x-component of the electric field under the gate is always smaller than the electron-velocity peak field E_p. The heating of electrons under the gate is thus negligibly small.

3) The carrier concentration changes gradually at the boundary of the depletion layer due to the diffusion effects. This distribution, is approximated by a sinusoidal function and a two-dimensional solution of Poisson's equation for the approximated carrier distribution is used. In this aspect our model is similar to one proposed by Yamaguchi and Kodera [3].

4) The drain current I_D is composed of two components - the channel current I_{ch} flowing through the channel and the Gunn domain, and a leakage current I_s in the non-ideal interface and substrate regions which have an effective shunt resistance. This feature is also similar to one considered by Engelmann and Liechti.

5) The ohmic resistances of the gate-source and gate-drain portions and contact resistances are considered in series with the channel and the Gunn domain.

The computation in the frame of this model involves only on iteration process to determine the field distribution under the gate and requires about 0.2 sec of computer time per point.

For the analytical description we have assumed that the current saturation occurs when the average electric field under the gate reaches the domain sustaining field

$$E_s = \frac{v_s}{\mu}$$

where v_s is the saturation electron drift velocity, μ is a low-field mobility. This assumption coupled with the Shockley theory leads to the following results. The channel current I_{ch} is almost linear up to the saturation point

$$I_{ch} \simeq g_0\left[1 - \frac{A_0}{A}\right]V_i = g_d V_i \qquad (1)$$

where

$$A_0 = \left[\frac{2\varepsilon_o\varepsilon(V_{Bi}-V_G)}{q\,N_D}\right]^{1/2} = A\left[\frac{V_{Bi}-V_G}{V_{po}}\right]^{1/2},$$

$$g_d \simeq g_o\left(1 - \frac{A_o}{A}\right)$$

(g_d is a drain conductance). The saturation current I_{sat} is equal to

$$I_{sat} = g_d V_s \; . \qquad (2)$$

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Here $V_s = E_s W_G$, $g_0 = \frac{q\mu N_D W A}{W_G}$, $V_{po} = \frac{q N_D A^2}{2 \varepsilon_o \varepsilon}$

V_{po} is a pinch-off voltage, q is the electronic charge, N_D is the doping density, $\varepsilon_o\varepsilon$ is the dielectric constant, A is the device thickness, W_G is the gate length, W is the gate width.

If $V_s << V_{Bi}-V_G$ (that normally takes place for GaAs MESFETs then the transconductance in the saturation region is

$$g_m \simeq g_o \frac{V_s}{2[V_{po}(V_{Bi}-V_G)]^{1/2}} = \left[\frac{q N_D \varepsilon_o \varepsilon_r}{2(V_{Bi}-V_G)}\right]^{1/2} \cdot v_s \cdot W \qquad (3)$$

We have also calculated the total charge under the gate and drain-to-gate and gate to source capacitances. If $V_s << V_{Bi}-V_G$ we have

$$Q = q N_D A_o W W_G \qquad (4)$$

$$C_{dg} \simeq C_{gs} \simeq \frac{1}{2\sqrt{2}} W W_G \left(\frac{\varepsilon_o \varepsilon q N_D}{V_{Bi}-V_G}\right)^{1/2} = \frac{1}{2}\frac{\varepsilon_o \varepsilon W W_G}{A_o} \qquad (5)$$

We defined a characteristic switching time of a GaAs MESFET as

$$\tau = \frac{Q(V_s)}{I_{sat}}$$

Using expressions (4) and (1) we get

$$\tau \simeq \frac{W_G}{v_s} \cdot \frac{A_o}{A-A_o} \qquad (6)$$

We see that the switching time is proportional to the transit time under the gate and that the saturation velocity rather than a peak velocity determines the switching time. But there are some physicaly limitations on the gate length which we analyzed.

The most important limitation is related to a stray capacitance and leads to the following criterion

$$W_G \geq A_o = \left[\frac{2 \varepsilon_o \varepsilon (V_{Bi} - V_G)}{q N_D}\right]^{1/2} \qquad (7)$$

For typical parameters of a GaAs MESFET the right-hand side of (7) is about 0.1 μm. That sets an ultimate limit for a characteristic switching time in a picosecond range (~2psec).

The power-delay product is equal to

$$P\tau \simeq q N_D W A_o W_G^2 E_s = W W_G^2 E_s \sqrt{2\varepsilon_o \varepsilon q N_D (V_{Bi}-V_G)}$$

This expression has a simple physical meaning. This is an amount of work to be done in order to move the total charge in the depletion layer ~ $q N_D W A_o W_G$ in the electric field E_s at the distance W_G.

The results of the calculations

Some of the results are depicted in Fig. 1-6 where the analytical calculation is compared with the computer calculation, with a rigorious computer analysis and with experimental data. This comparison shows a good agreement.

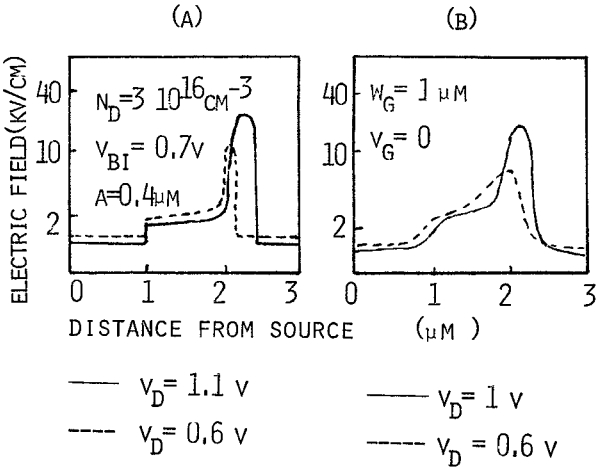

FIG. 1 - ELECTRIC FIELD DISTRIBUTION IN GAAS MESFET.
(A) PRESENT COMPUTER MODEL
(B) COMPUTER ANALYSIS OF YAMAGUCHI AND KODERA

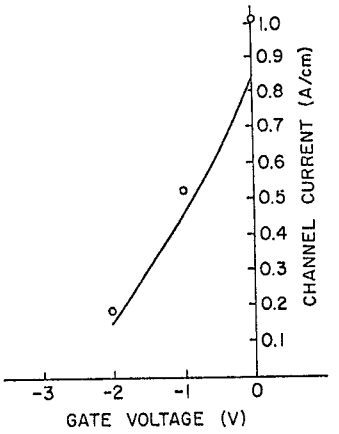

FIG. 2 - CHANNEL SATURATION CURRENT VERSUS GATE VOLTAGE.
SOLID LINE - OUR ANALYTICAL MODEL
CIRCLES - COMPUTER ANALYSIS OF YAMAGUCHI & KODERA
PARAMETERS ARE THE SAME AS FOR FIG. 1.

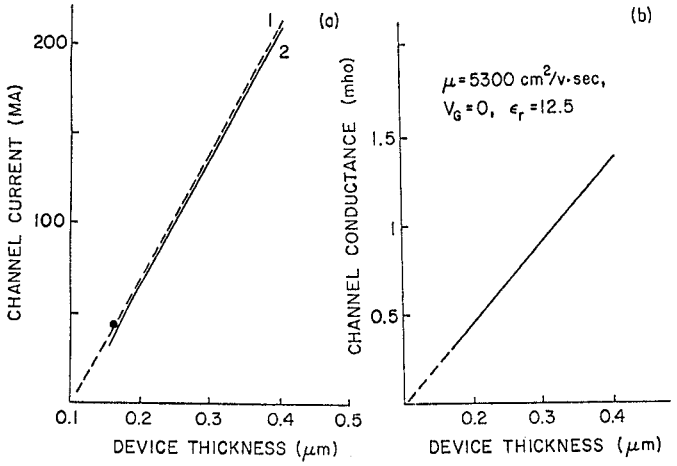

FIG. 3 - CHANNEL SATURATION CURRENT (A) AND CHANNEL CONDUCTANCE (B) VERSUS DEVICE THICKNESS.
$N_D = 1.1 \times 10^{17}$ cm^{-3}, $V_{BI} = 0.8$V, $W_G = 1$ μM, $W = 500$ μM, $V_s = .8 \times 10^7$ cm/sec.

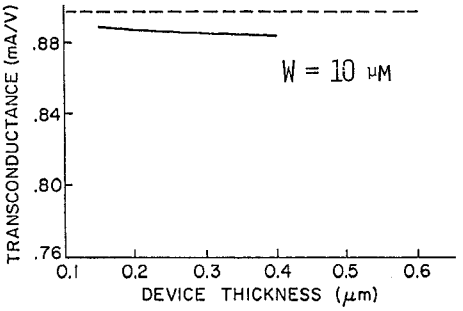

FIG. 4 - TRANSCONDUCTANCE VERSUS DEVICE THICKNESS.

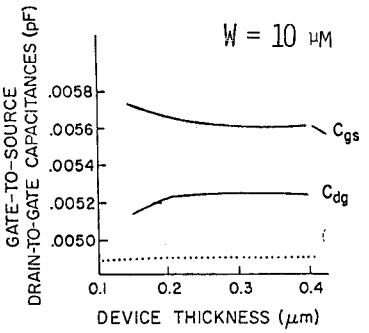

FIG. 5 - GATE-TO-SOURCE AND DRAIN-TO-GATE CAPACITANCES VERSUS DEVICE THICKNESS.

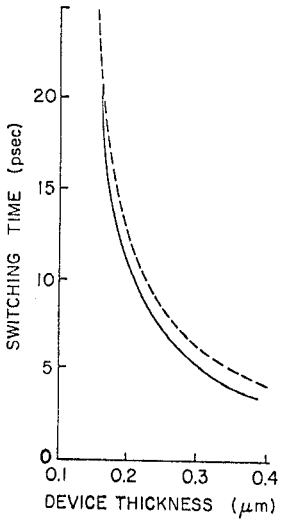

FIG. 6 - SWITCHING TIME VERSUS DEVICE THICKNESS.

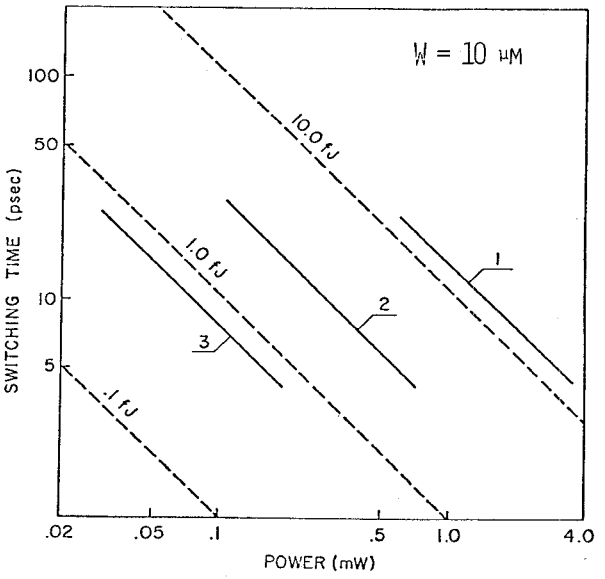

FIG. 7 - SWITCHING TIME VERSUS POWER FOR GaAs MESFETs.

For Fig. 3-7 dashed lines represent our analytical results; solid lines represent our computer calculation.

Conclusion

Our results show that GaAs MESFETs can yield a power-delay product in femto-joule range in good agreement with experimental data.

References

1. Gelmont, B.L. and Shur, M.S., "Analytical theory of stable domains in high-doped Gunn diodes," Electron. Lett., vol. 6, pp. 385-387, 1970.
2. Engelmann, R.W.H. and Liechti, C.A., "Gunn domain formation in the saturated current region of GaAs MESFET's," IEDM Tech. Dig., pp. 351-354, Dec. 1976.
3. K. Yamaguchi and H. Kodera, "Drain conductance of junction gate FET's in the hot electron range," IEEE Trans. Electron Devices, vol. ED-23, pp. 545-553, June 1976.